SECTOR
UPDATE

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Tech (OVERWEIGHT)

Computex 2026: Nvidia reasserts leadership

- This year's Computex stood out because even Nvidia showcased integrated solutions for agentic AI, alongside new CPUs and PCs, revealing that the warmth of AI is extending beyond GPUs.
- While many companies have recently been re-evaluated through the lens of AI, Nvidia's business opportunities are likely to expand further with the upcoming launch of the Vera-Rubin platform in 2H, renewing interest in the existing Nvidia value chain.

WHAT'S THE STORY?

At Computex 2026, what changed? While attention had previously focused solely on Nvidia's GPU value chain, this year interest broadened across the entire server ecosystem—not just the GPU.

- **CPU:** The unifying theme of Nvidia's keynote was agentic AI. Within this context, significant time was devoted to the Vera CPU. Whereas CPUs in past AI servers merely issued commands to GPUs, they now play expanded roles—including KV cache management, software control, orchestration, data access, security, and storage.
- **Connectivity:** The bottleneck in AI is shifting from "how fast computation and memory can perform" to "how much data can be connected, and how quickly and broadly it can be transmitted." To achieve higher bandwidth and longer transmission distances, the transition from copper to optical interconnects is becoming inevitable—so much so that Jensen Huang has positioned Marvell as a potential next trillion-dollar company.
- **Memory:** All three memory leaders are prominently showcasing their next-generation HBM products. Samsung Electronics (SEC), in particular, unveiled a prototype of HBM5—the next-next-generation—to signal aggressive participation in the competition. The trend toward higher-capacity SOCAMMs, combined with growing demand from RTX Spark and robotics applications, confirms a broadening base of AI memory demand. We view concerns about supply oversupply before 2028 as premature, supported by SK Chairman Chey Tae-won's pledge to double wafer capacity within five years.
- **CCL & substrates:** The adoption of Vera Rubin's midplane architecture and SOCAMM2 is expected to expand the TAM for CCL and substrates. Doosan Corp, a supplier of low-loss CCL for AI servers, and Simmtech, which provides module PCBs and MCP substrates for SOCAMM, are well-positioned to benefit from this structural shift.

(Continued on the next page)

Investment strategy – Expect renewed interest in Nvidia's value chain in 2H: This year, AI's warmth has broadened, and stocks traditionally seen as unrelated to AI—like Intel—have outperformed. While the universe of AI beneficiaries has expanded, Nvidia and its value chain (memory chipmakers and TSMC) continue to dominate the AI hardware market and hold the strategic leverage in the ecosystem. The launch of the Vera-Rubin platform (encompassing CPUs, LPX, and more) in 2H marks a new inflection point. As Nvidia's business opportunities expand and it captures new segments of the market, its value chain will also benefit. We anticipate renewed interest in existing Nvidia value chain.

Rise of agentic AI expands role of CPUs (Feat. Nvidia)

This year at Computex, Nvidia and Jensen Huang once again dominated the spotlight, with Huang reaffirming his role as a leading evangelist for AI. The keynote's central theme was agentic AI—how it is transforming data center architectures and Nvidia's strategic response.

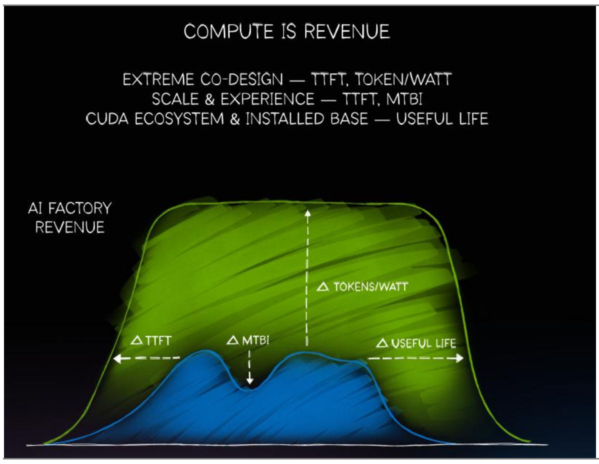
The equation 'Compute = Revenue' remains foundational to Nvidia. The core of AI monetization hinges on three factors: 1) how quickly the first token can be generated after system deployment; 2) maximizing token throughput within limited power budgets; and 3) the operational lifespan of the deployed system. Nvidia has consistently emphasized that it's not the upfront cost of building a system that matters—but its total cost of ownership (TCO). What truly defines competitiveness is the ability to generate more tokens, faster—even at a higher cost—and running the system reliably for years.

The operational model of data centers in the LLM era differs fundamentally from data centers required for agentic AI. In the LLM era, CPUs primarily served to manage GPU, which handled all the computations. But as inference becomes more complex and agentic AI scales, relying solely on GPUs for all tasks has become inefficient—and inefficiency directly translates to lower token throughput and reduced revenue

Agentic AI operates autonomously and continuously through multiple sequential stages: setting goals, planning, executing, retrieving data, invoking tools, validating results, and iterating. These tasks rely less on massive matrix operations (GPU's strength) and more on fast, sequential processing, which is where CPUs excel. While GPUs remain essential for heavy parallel computation, the orchestration layer between GPU tasks is increasingly handled by CPUs.

Nvidia unveiled its Vera CPU, purpose-built for agentic AI. Built with 88 custom Arm-based cores, Vera CPU delivers three times the bandwidth per core and twice the total bandwidth compared to traditional x86 CPUs. In Python-based workloads, Vera CPU demonstrated 1.8x better performance than traditional x86 designs. With Vera, Nvidia has begun selling CPUs independently—perhaps signaling a shift in strategy. While the company until last year emphasized coexistence and open ecosystems with other semiconductor firms, it now appears to be reasserting its competitive edge.

Compute = Revenue

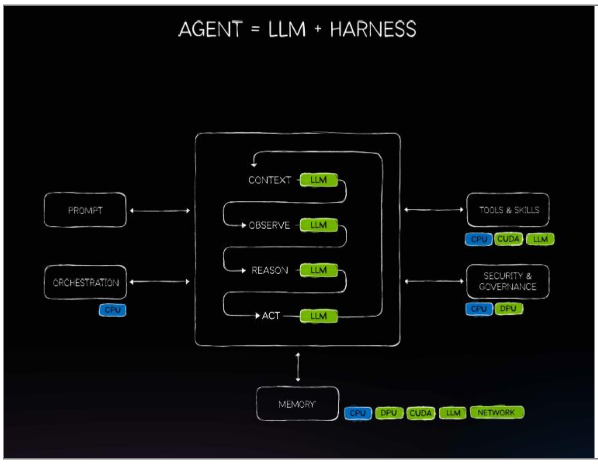


COMPUTE IS REVENUE

EXTREME CO-DESIGN — TTFT, TOKEN/WATT
SCALE & EXPERIENCE — TTFT, MTBI
CUDA ECOSYSTEM & INSTALLED BASE — USEFUL LIFE

Source: NVIDIA, Samsung Securities

Task allocation among agentic AI



AGENT = LLM + HARNESS

Source: NVIDIA, Samsung Securities

Three rack solutions have been introduced based on the Vera CPU. The first is the Vera-Rubin rack, which builds upon the legacy of the Grace-Blackwell series. Like its predecessor, this rack is designed for large-scale LLM training and high-performance inference—workloads that rely heavily on GPU computation. In this configuration, the CPU's role remains unchanged: it simply manages GPU operations.

The second solution is Vera Compute—a rack composed entirely of CPUs, with no GPUs. As previously noted, the diverse orchestration layers required by agentic AI are inherently CPU-intensive, making Vera Compute a purpose-built architecture for these workloads.

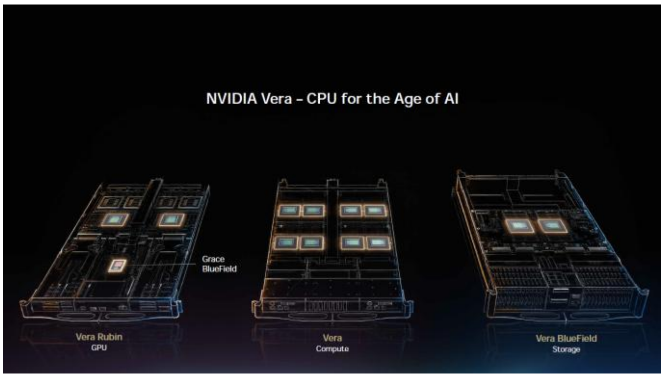
The third solution is Vera BlueField, specialized for storage. Agentic AI repeatedly reads and writes massive volumes of context—a process that demands both high throughput and robust security. To meet these needs, Vera BlueField pairs the Vera CPU with the BlueField DPU dedicated to offloading workloads involving data movement, storage, and security.

While the spotlight has fallen on the Vera CPU and its competitive performance, there is a risk of misinterpreting this as a diminished role for GPUs. In reality, all three new solutions are ultimately designed to serve the GPU. The data center architecture is evolving to distribute workloads more effectively, allowing GPUs to focus solely on token generation—the revenue driver. The process is simply elevating the CPU's role and importance.

The key point is that as generative AI scales, the CPU's role is growing—and Nvidia's business opportunities are rapidly expanding as a result. Vera-Rubin has already entered mass production and is scheduled for shipment starting in 3Q. Alongside Vera-Rubin, multiple new products—including Vera CPU, Groq LPU, and Bluefield—are poised for launch. Notably, during the last earnings call, the company provided guidance that Vera CPU standalone sales could reach USD20b this year.

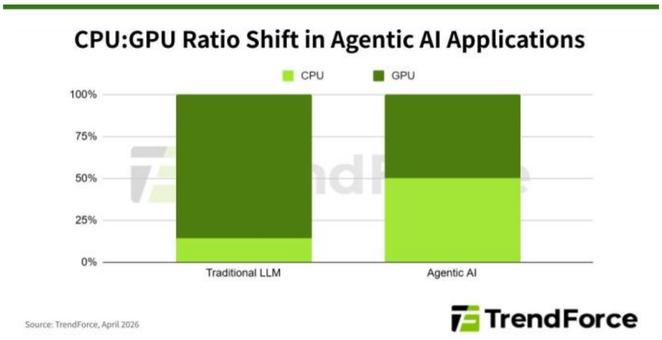
Meanwhile, Jensen Huang has formally entered the PC CPU market alongside agentic AI, reaffirming that ‘on-device AI’ remains a vital goal. He unveiled the RTX Spark, an AI laptop co-developed with Microsoft. It combines a N1 series CPU (with 20 Grace cores; co-developed with MediaTek), a Blackwell GPU, and up to 128GB of unified memory. Huang argued that individual consumers will soon rely on AI agents—and that traditional PCs must be fundamentally reimagined. He stressed that, unlike current AI PCs that depend solely on NPU cores added to the CPU, true AI performance at the edge requires much stronger local computing power—just as GPUs revolutionized AI servers. Like the DGX Spark workstation introduced earlier, the immediate market may be small—but the significance lies in the sustained effort to bring AI into the PC edge.

Vera CPU’s 3 applications


NVIDIA Vera – CPU for the Age of AI

Source: NVIDIA, Samsung Securities

CPU: GPU ratio shift in agentic AI applications


CPU:GPU Ratio Shift in Agentic AI Applications

Source: TrendForce, April 2026

Source: Trendforce, Samsung Securities

The third bottleneck in AI infrastructure: Connectivity

At Computex 2026, Jensen Huang made a surprise appearance at Marvell's keynote, naming Marvell a potential future trillion-dollar company. The core rationale lies in the shifting bottleneck of AI infrastructure—from compute and memory to connectivity. Until now, competition in AI has centered on GPU computational performance and HBM bandwidth.

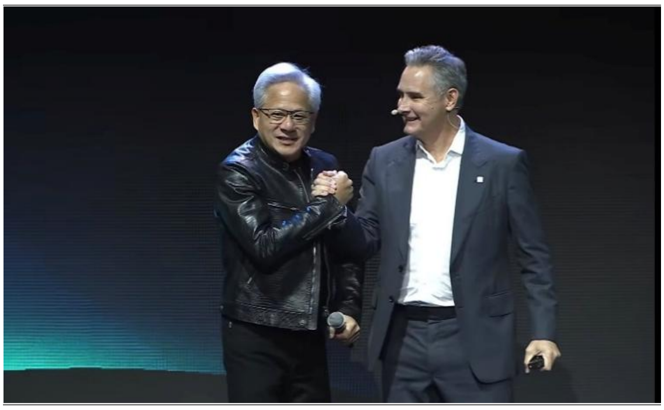
However, as AI models evolve toward inference, Mixture-of-Experts (MoE), and agentic AI, the ability to integrate tens of thousands—and eventually millions—of processors into a unified, high-performance engine has become more critical than raw chip-level compute power. The focus is no longer merely "how fast a single unit can calculate," but "how quickly and efficiently vast amounts of data can be interconnected." Marvell defines this shift as the third bottleneck in AI infrastructure: Connectivity.

The central challenge in overcoming this bottleneck is the transition from copper to optical interconnects. Copper suffers from a fundamental physical limitation: as data rates increase, transmission distance sharply decreases. This limit is known as the "Copper Wall." To overcome it, optical solutions—though more expensive—are required. In current 200 Gbps/lane environments, copper cable length is restricted to approximately 2.5 meters. At 400 Gbps, even connecting across a single 2-meter-high rack becomes challenging. As a result, the Copper Wall, once confined to inter-rack (scale-out) distances, is now moving inward into intra-rack (scale-up) spaces.

Marvell has explained that each time the Copper Wall moves to a shorter distance domain, the number of required connections increases by roughly tenfold. When optics penetrate deep into the rack, demand for optical components grows not just proportionally, but exponentially. The key enabling technology here is Co-Packaged Optics (CPO), which places optical components directly adjacent to the silicon chip, pulling optical connectivity into the heart of the rack. This drives demand across the entire optical supply chain—optical components, packaging, testing, and back-end processing. This transition is not merely a component upgrade—it represents a structural transformation of expanding the supply chain and ecosystem.

Amid this transformation, Marvell is poised to be redefined not as a secondary player in ASIC and networking markets, but as the leading Connectivity Platform for AI infrastructure. Its unique positioning— being responsible for every connection in AI infrastructure—from long-distance inter-datacenter links to chiplet-level connections within a package—should become increasingly prominent.

Nvidia CEO Jensen Hwang and Marvell CEO Matt Murphy



Source: Computex 2026

The third bottleneck in AI infrastructure, connectivity

Connectivity: The new defining challenge of AI

Compute

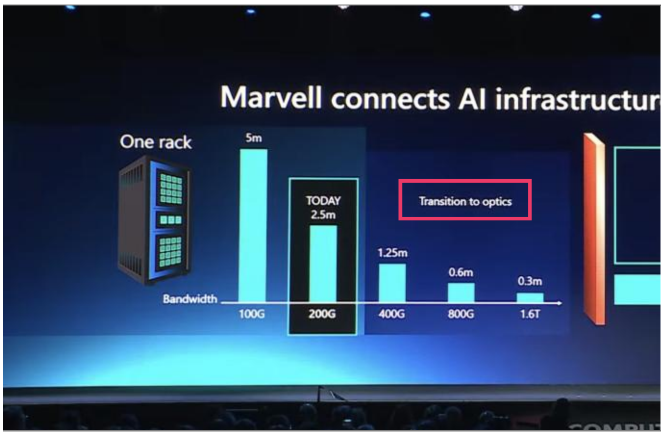
Memory

Connectivity

Bottleneck

Source: Computex 2026

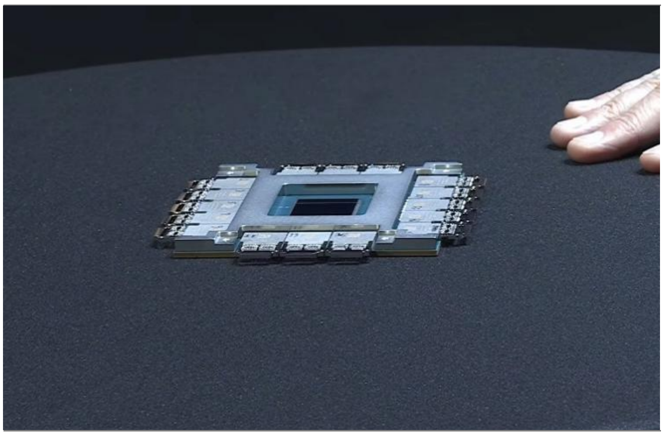
The transition to optics begins at 400G



Marvell connects AI infrastructur

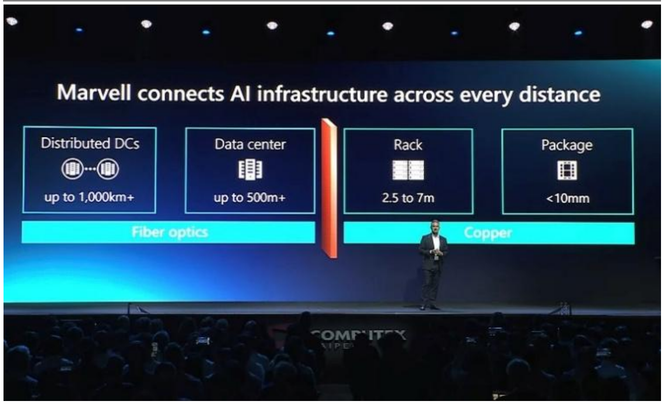
Source: Computex 2026

Marvell: 51.2T CPO-based switch



Source: Computex 2026

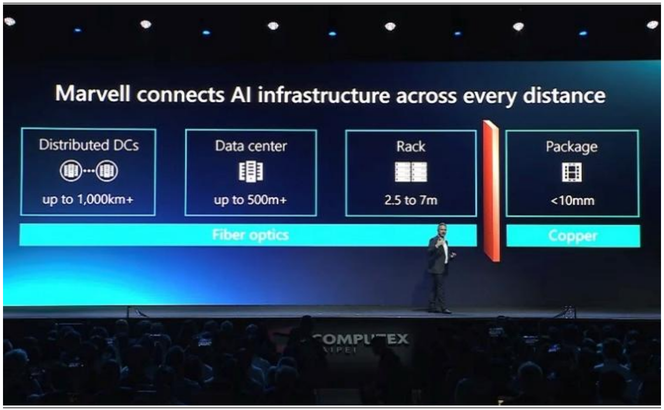
The copper wall in scale-out networks



Marvell connects AI infrastructure across every distance

Source: Computex 2026

The copper wall in scale-up networks



Marvell connects AI infrastructure across every distance

Source: Computex 2026

Marvell's core technologies across connectivity distances

Segment	Distance	Purpose	Core technology	Current status
Scale-across (Inter-datacenter)	Hundreds of km	Long-haul connectivity between data centers	Coherent modulation, Coherent DSP, Long-reach optics	800G currently in volume production; 1.6T 2nm-based products expected to begin sampling by year-end
Scale-out (Intra-datacenter)	Hundreds of meters	Connectivity for rack, spine, and switch networks	PAM4 DSP, TIA, Laser driver, Ethernet switching	1.6T 3nm PAM products ramped last year; 12.8T-51.2T switch portfolio available; 100T Ethernet switch announced
Scale-up (Intra-rack)	Several meters	GPU/XPU interconnects	Electrical SerDes, Copper backplane, Scale-up switch	Still dominated by copper interconnects; 200G SerDes portfolio available; 400G SerDes planned
In-package	Several mm²	Chiplet die-to-die connectivity	Die-to-die SerDes, 2.5D/3D packaging	Supports the design of complex chiplet architectures

Source: Marvell, Samsung Securities

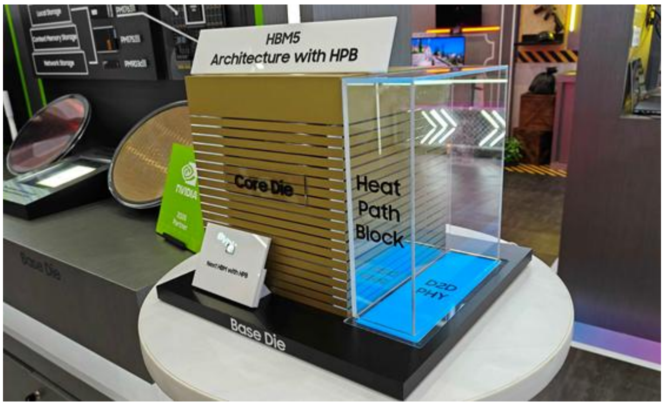
Applications of AI memory are broadening amid intense competition in HBM technology

The race in HBM technology is already racing toward the next generation. At Computex 2026, Samsung Electronics (SEC) unveiled its first prototype of the 8th-generation HBM5, featuring a 2nm base die, a Heat Path Block (HPB) thermal architecture, pin speeds up to 16 Gbps, a total bandwidth of 4 TB/s, and stacking configurations of 12H, 16H, or 20H—mass production is expected after 2028. SK Hynix displayed its first HBM4E wafer samples, and Jensen Huang notably left the comment "Please Make More," underscoring the urgency of supply. Micron Technology also showcased its HBM4 36GB 12H product, confirming its entry into the next-generation HBM competition.

Nvidia announced at Computex that its RTX Spark platform will feature a 128GB SOCAMM module. SK Hynix revealed a 192GB SOCAMM, while Micron unveiled a 256GB SOCAMM2. If the era of personal AI agents emerges and HPC-grade devices replace traditional laptops in daily use, the average content memory per device is expected to surge from today's typical 12GB to over 128GB. This signals a structural shift: the mainstream of server DRAM is moving toward low-power, high-density LPDDR, and demand is no longer confined to data centers—it is expanding into robotics, edge devices, and consumer HPC systems.

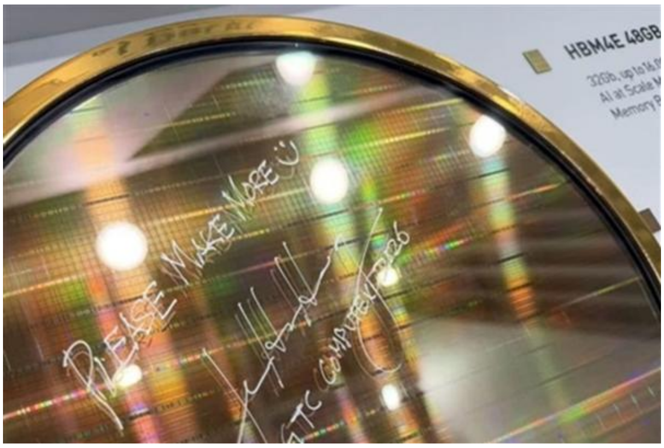
SK Group Chairman Chey, Tae-won warned at Computex that HBM supply shortages will persist until 2030, and pledged to double wafer capacity within five years. We agree with this assessment. Even as new fabs begin contributing to supply starting in 2027, the industry's true "new normal" capex scale should only become visible after 2029, when both fabs in the Yongin cluster reach full ramp-up. Delaying this acceleration until after 2029 itself signals that supply oversupply is unlikely before 2028.

Samsung Electronics' HBM5 mock-up



Source: Press release

Jensen Hwang "Please make more"



Source: Press release, Samsung Securities

Expanding the CCL TAM through midplane adoption

At Computex 2026, the Vera Rubin platform—first unveiled at CES 2026—was prominently highlighted once again. The core innovation of Vera Rubin lies in its reimagined server interconnect architecture. While the previous Blackwell platform relied on a cable-based topology, Vera Rubin introduces a cableless compute tray architecture centered on a central midplane PCB.

In Blackwell systems, GPUs, NICs, and storage were connected via numerous cables. However, as GPU counts increased and NVLink bandwidth expanded, the sheer volume of cables led to escalating assembly complexity and growing challenges in signal integrity. During his keynote at Computex 2026, Jensen Huang publicly unveiled a midplane prototype and identified it as one of the defining changes in the Vera Rubin architecture.

The adoption of a midplane architecture is not merely a component substitution—it replaces the signal transmission function previously handled by cables with a large-scale printed circuit board (PCB). The midplane serves as a centralized, high-density interconnect substrate that links 18 compute trays and 9 NVLink switch trays. This concentrates massive high-speed signals onto a single PCB, driving demand for larger board areas, higher layer counts, and greater adoption of low-loss dielectric materials.

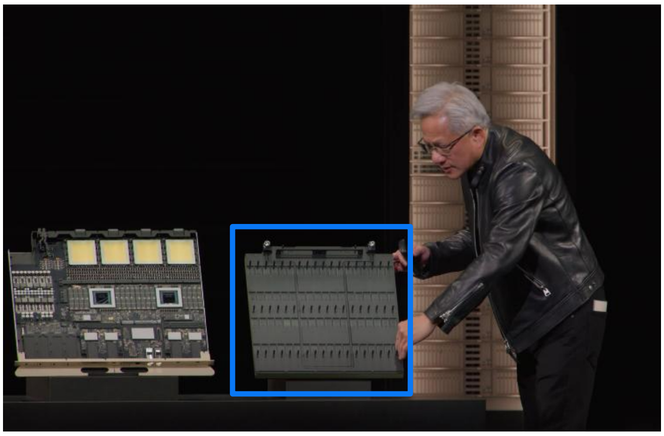
We expect this shift to significantly expand the total addressable market (TAM) for high-performance copper-clad laminates (CCL). Vera Rubin marks the beginning of a new TAM category: the midplane itself. Based on our analysis, CCL demand per rack under Vera Rubin is projected to increase by approximately 1.5x compared to the GB300 platform. In Korea, Doosan Corp is positioned as the most likely primary beneficiary. As a key CCL supplier for Nvidia's compute trays in the Blackwell architecture, Doosan is well-placed to extend its existing supply relationship into Vera Rubin.

The SOCAMM market opens up

The most significant innovation in Vera CPU is the adoption of SOCAMM2. Jensen Huang described the market potential of Vera CPU as a "multi-billion-dollar business." We believe that as GPU counts in AI servers continue to grow, the CPU's orchestration role—managing data movement and resource allocation—will become even more critical. We expect the substrate market for SOCAMM to expand significantly as Vera CPU adoption accelerates.

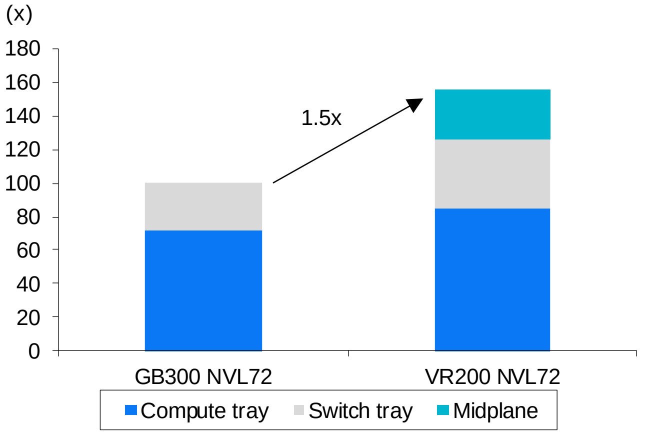
The key structural change in substrates lies not merely in increased memory capacity, but in the modular design of SOCAMM2. Unlike traditional memory configurations, SOCAMM2 integrates multiple LPDDR dies onto a single module PCB, creating entirely new substrate demand. Furthermore, within each LPDDR package, high-performance Multi-Chip Package (MCP) substrates are also used, driving simultaneous growth in demand for both the module PCB and the underlying MCP substrate. In Korea, Simmtech and TLB are expected to be the primary beneficiaries. Simmtech, in particular, has secured first-vendor status across all three major memory suppliers' SOCAMM supply chains. We anticipate Simmtech to capture over 50% of the SOCAMM substrate market share.

Midplane introduced with Vera Rubin



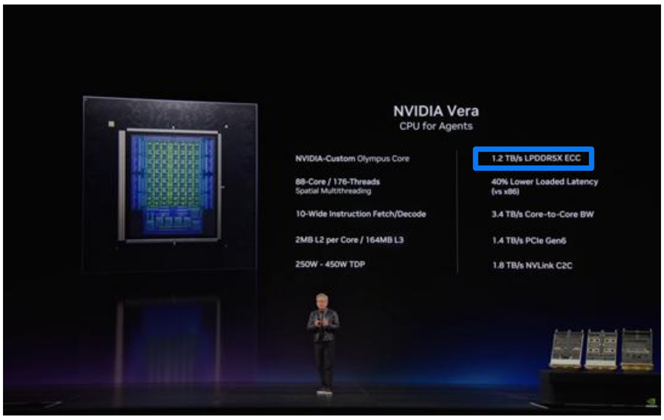
Source: NVIDIA, Samsung Securities

Growing CCL demand in Vera Rubin



Source: Samsung Securities estimates

Vera CPU specs unveiled



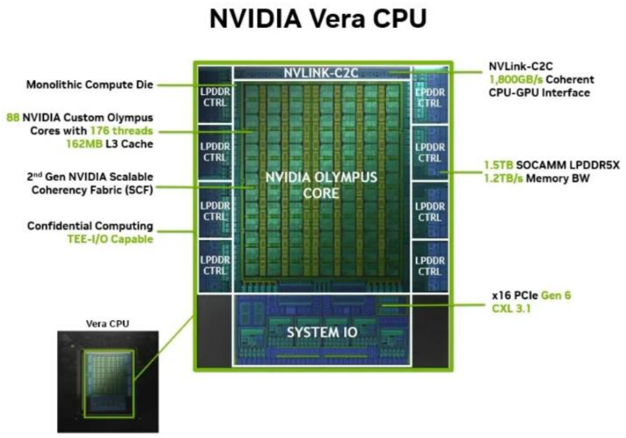
NVIDIA Vera
CPU for Agents

NVIDIA-Custom Olympus Core
88-Core / 176-Threads
Spatial Multithreading
10-Wide Instruction Fetch/Decode
2MB L2 per Core / 164MB L3
250W - 450W TDP

1.2 TB/s LPDDR5X ECC
40% Lower Loaded Latency (vs x86)
3.4 TB/s Core-to-Core BW
1.4 TB/s PCIe Gen6
1.8 TB/s NVLink C2C

Source: NVIDIA

Vera CPU architecture



Source: NVIDIA

Investment strategy – Expect renewed interest in Nvidia's value chain in 2H

Excluding memory, many of the top-performing stocks in the global tech sector this year were companies that previously had little to do with AI—only to be reclassified as AI beneficiaries as the broader AI momentum finally reached them.

A prime example is Intel. Once seen as lagging in the AI accelerator race—especially GPUs—and labeled as legacy or non-AI players, Intel faced little growth expectation in an environment where all capital flowed exclusively toward AI. But with the surge in inference demand and the rise of agentic AI, CPUs have emerged as core semiconductors in AI data centers—leading to a renewed evaluation of Intel.

When corporate perceptions shift, valuation multiples adjust accordingly. And since such shifts are typically grounded in revised outlooks, stock prices can rise rapidly. As the AI cycle extends, the universe of AI beneficiaries continues to expand (as was the case with Intel), and markets naturally gravitate toward new faces.

Yet, as evident even at this year's Computex, Nvidia and its value chain (including memory and TSMC) continue to set the direction for AI data centers and hold the dominant position in the ecosystem. For this reason, we expect the launch of the Vera-Rubin platform in 2H to serve as another pivotal inflection point. Unlike prior generations, the market scope targeted by Nvidia with Vera-Rubin has significantly broadened, and products like the Vera CPU are already delivering tangible results. We believe it is essential to focus on the upside potential of Nvidia's upcoming product releases, and reaffirm that Nvidia remains the core stock in the global semiconductor sector.

As Nvidia's business opportunities expand and it captures new segments of the market, it is natural that its value chain also benefits. Standing to gain again are: 1) TSMC, which handles the production and advanced packaging for nearly all of Nvidia's products; and 2) memory suppliers (Samsung Electronics, SK Hynix, Micron), whose high-value-added product mix will grow with the transition to HBM4 and adoption of SOCAMM in the Vera-Rubin generation.

While this dynamic may naturally lead investors to extend their focus to TSMC and memory players' value chain, our priority remains on those most directly and immediately exposed to Nvidia's new product cycle: TSMC and memory suppliers.

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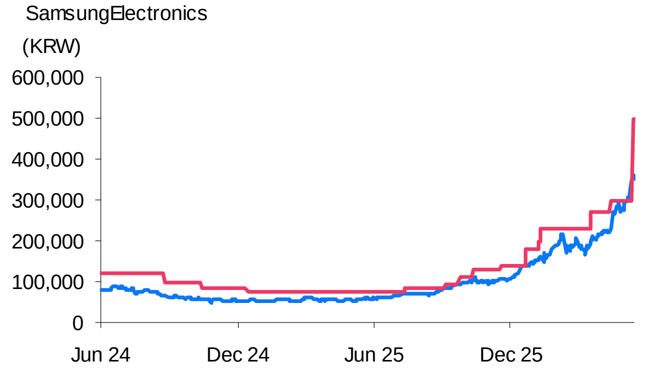
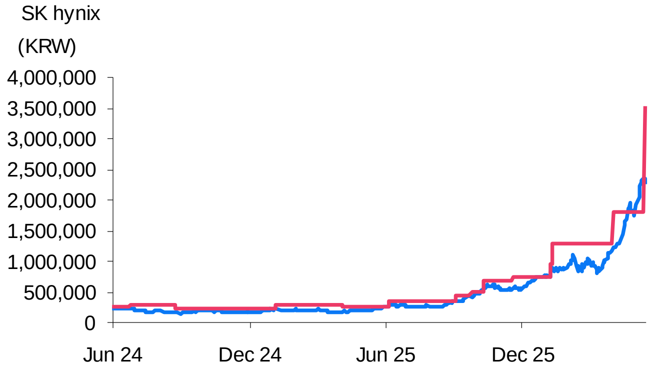
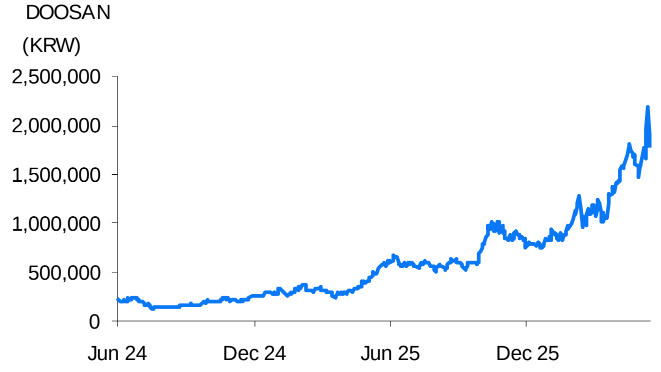
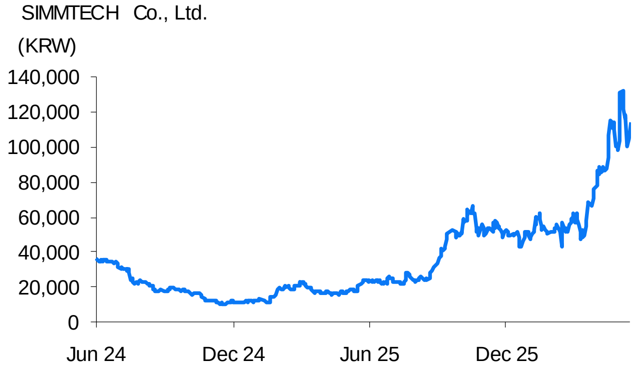
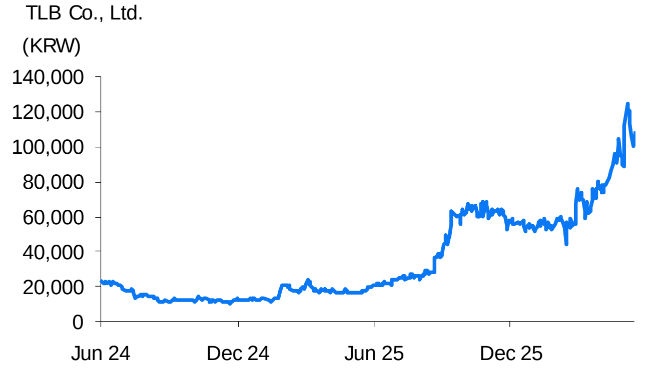
Target price changes in past two years











Rating changes over past two years (adjusted share prices)

SamsungElectronics

Date	2024/5/28	9/12	11/1	2025/1/2	8/1	9/23	10/13	10/31	12/8	2026/1/9	1/27	1/30	4/7	5/4	6/2
Recommendation	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY
Target price (KRW)	120000	100000	83000	74000	85000	93000	110000	130000	140000	180000	200000	230000	270000	300000	500000
Gap* (average)	-34.45	-39.49	-33.92	-21.93	-15.05	-6.95	-10.64	-21.96	-16.54	-18.69	-19.23	-19.75	-20.25	-3.39	
(max or min)**	-26.83	-35.30	-29.28	-1.89	-1.76	1.51	-5.36	-14.54	0.71	-15.39	-18.80	-5.22	-16.30	16.33	

SK hynix

Date	2024/4/8	7/12	9/12	2025/1/24	4/24	6/25	9/23	10/13	10/30	12/8	2026/1/27	1/30	4/21	6/2
Recommendation	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY	BUY
Target price (KRW)	250000	280000	240000	280000	250000	340000	430000	500000	700000	750000	950000	1300000	1800000	3500000
Gap* (average)	-18.91	-34.15	-23.78	-30.26	-14.53	-17.52	-14.81	-3.33	-19.05	-11.48	-10.42	-26.68	-3.42	
(max or min)**	-3.60	-16.79	-6.04	-21.96	11.40	3.82	-0.47	11.60	-11.43	2.27	-9.37	-10.31	31.28	

DOOSAN

Date	2026/6/5
Recommendation	Not Rated
Target price (KRW)	n/a
Gap* (average)	
(max or min)**	

SIMMTECH Co., Ltd.

Date	2026/6/5
Recommendation	Not Rated
Target price (KRW)	n/a
Gap* (average)	
(max or min)**	

TLB Co., Ltd.

Date	2026/6/5
Recommendation	Not Rated
Target price (KRW)	n/a
Gap* (average)	
(max or min)**	

Note: * [(average, maximum, or minimum share price over duration of target price minus target price) / target price] x 100%
** Maximum/minimum share price if new target is higher/lower than market close on the business day prior to target price change

Samsung Securities uses the following investment ratings*

Company

BUY	Expected to increase in value by 15% or more within 12 months and is highly attractive within sector
HOLD	Expected to increase/decrease in value by less than 15% within 12 months
SELL	Expected to decrease in value by 15% or more within 12 months

Industry

OVERWEIGHT	Expected to outperform market by 5% or more within 12 months
NEUTRAL	Expected to outperform/underperform market by less than 5% within 12 months
UNDERWEIGHT	Expected to underperform market by 5% or more within 12 months

* Note: Effective Jul 27, 2023, BUY, HOLD, and SELL criteria are based on expectations of share-price moves of 15% or more within 12 months

Percentage of ratings in 12 months prior to 2026.03.31

BUY(85.2%)·HOLD(14.8%)·SELL(0%)

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General

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